

REMARKS

This application has been carefully reviewed in light of the Office Action dated July 29, 2005. Claims 1 to 16 are now pending in the application, with Claims 11 to 16 having been newly-added herein. Claims 1, 5, 6, 10 and 13 to 15 are the independent claims herein. Reconsideration and further examination are respectfully requested.

Figure 7 of the drawings was objected to for not including a Prior Art legend. A Replacement Sheet for Figure 7, which includes a Prior Art legend, is being submitted herewith and approval thereof is respectfully requested.

Claims 1 to 10 were rejected under 35 U.S.C. § 112, second paragraph. Applicants note that, while the claims were alleged to be unclear, the Examiner's general understanding of the claimed invention as set out in the § 112 rejections is correct. Accordingly, without conceding the correctness of the rejections, the claims have nonetheless been amended giving due consideration to the points noted in the Office Action so as to make the claimed subject matter even clearer. Thus, reconsideration and withdrawal of the rejections are respectfully requested.

Claims 1, 2, 4, 6 and 7 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,961,616 (Wakasugi), Claims 3, 5, 8 and 10 were rejected under 35 U.S.C. § 103(a) over Wakasugi in view of U.S. Patent No. 6,570,666 (Sotokawa), and Claim 9 was rejected under § 103(a) over Wakasugi in view of U.S. Patent No. 6,175,603 (Chapman). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention generally relates to filtering noise in input information. According to the invention, a first circuit (which may comprise an interface connector and a glitch noise filter) detects whether there is a change in first input information (e.g., information input from an external apparatus), and if so, second input

information (e.g., input information in which noise has been removed) is fetched (latched) after an elapse of a predetermined time. Then, a second circuit (e.g., a logical filter) determines whether the fetched information matches a protocol of the first input information, and if not, the fetched information is skipped.

Referring specifically to the claims, amended independent Claim 1 is an interface apparatus for inputting information from an external apparatus, comprising a first circuit for, in a case where there is a change in first input information, fetching second input information after an elapse of a predetermined time, and a second circuit for, when the second input information fetched by the first circuit is not matched with a protocol of the first input information, skipping the fetched information according to the protocol.

Amended independent Claim 6 is a method claim that substantially corresponds to Claim 1, Claim 5 is directed to a printer that includes features substantially corresponding to those of Claim 1, and Claim 10 is a method claim that substantially corresponds to Claim 5.

Newly-added independent Claim 13 is directed to substantially the same invention as Claim 1, but includes additional details. Thus, Claim 13 is an interface apparatus for inputting information from an external apparatus, comprising a change detector for detecting a change in first input information and outputting a reset upon the detection of the change, a timer for inputting the reset output by the change detector and outputting a trigger after an elapse of a predetermined time from the input of the reset, a latch for inputting the trigger output by the timer and fetching second input information upon the input of the trigger, and a logical filter for, when the second information fetched by the latch is not matched with a protocol of the first input information, skipping the fetched information.

Newly-added Claim 14 is along the lines of Claim 13, but with one difference being that the logical filter in which, when the second information fetched by the latch is matched with a protocol of the first input information, outputs the fetched information.

Amended independent Claim 15, while being directed to the same invention as the foregoing independent claims, is nonetheless directed to an interface apparatus for inputting information from an external apparatus, comprising a timer for timing a predetermined time, and a comparator for making a comparison between a length of a low level state in input information within the predetermined time timed by the timer, and a length of a high level state in the input information within the predetermined time, and for outputting a low level signal if the comparison shows that the length of the low level state is longer than the length of the high level state, and outputting a high level signal if the comparison shows that the length of the high level state is longer than the length of the low level state.

The applied art, alone or in any permissible combination, is not seen to disclose or to suggest the features of the present invention. In particular, with regard to Claims 1, 5, 7 and 10, the applied art is not seen to disclose or to suggest at least the feature of a second circuit for, when second input information, that is fetched by a first circuit after a predetermined time has elapsed in a case where there is a change in first input information, is not matched with a protocol of the first input information, skipping the fetched information according to the protocol.

Wakasugi shows a data transfer system that includes a host and a peripheral device in which the host transfers a timing signal (host strobe signal) and data to the peripheral device. The peripheral device detects a change in the received transferred data,

resets a counter responsive to the detection of data change, and then sends an internal strobe signal to a data receive circuit after the lapse of a predetermined time. This structure allows the peripheral device to latch the received transferred data in response to the internal strobe signal, even if the host strobe signal is absent. Wakasugi is completely silent, however, as to the claimed second circuit. In this regard, Wakasugi latches the input data in response to the internal strobe signal, and uses the latched data even if that data is not matched with a protocol of the data from the host. Thus, Wakasugi does not check such matching of the protocol as claimed, or skipping of the data that does not match the protocol. Accordingly, Claims 1 and 6 are not believed to be anticipated by Wakasugi.

Claim 5 is directed to a printer that comprises the first and second circuits recited in Claim 1, together with a printer engine, and Claim 10 recites a corresponding method claim. Since Wakasugi fails to teach the second circuit as discussed above, it fails to anticipate Claims 5 and 10.

As for Sotokawa, it is not seen to make up for the foregoing deficiencies of Wakasugi. In this regard, even if Sotokawa were seen to disclose all that it is cited for (i.e., that data is printed if it matches a protocol), such a feature nonetheless fails to read on, or suggest, the feature of skipping of the data that does not match the protocol. Accordingly, Claims 5 and 10 are believed to be allowable over Wakasui and Sotokawa.

Turning to newly-added Claim 13, it includes a change detector, a timer, a latch and a logical filter. The change detector detects a change in first input information and outputs a reset upon the detection of the change. The timer inputs the output reset and outputs a trigger after an elapse of a predetermined time from the input of the reset. The latch inputs the output trigger and fetches second input information upon the input of the trigger. When the fetched information is not matched with a protocol of the first input

information, the logical filter skips the fetched information. Claim 14 is identical to claim 13 except that when the fetched information is matched with the protocol, the logical filter outputs the fetched information.

Similar to Claims 1, 5, 6 and 10, the art of record is not seen to disclose or to suggest the features of Claims 13 and 14, and in particular is not seen to disclose or to suggest at least the feature of a logical filter for, when second information fetched by a latch is not matched with a protocol of first input information, skipping the fetched information.

As discussed above, both Wakasugi and Sotokawa fail to teach or suggest the claimed logical filter. Thus, Claims 13 and 14 are therefore believed to be allowable.

Newly-added Claim 15 recites an interface apparatus for inputting information from an external apparatus, comprising a timer and a comparator. The comparator makes a comparison between a length of a low level state in input information within a predetermined time set by the timer, and a length of a high level state in the input information within the predetermined time. If the comparison shows that the length of the low level state is longer than that of the high level state, the comparator outputs a low level signal, and if not, the comparator outputs a high level signal.

The foregoing features of Claim 15 are not believed to be disclosed by, or suggested by the art of record, and in particular, the art of record is not seen to disclose or to suggest at least the feature of a comparator for making a comparison between a length of a low level state in input information within a predetermined time timed by a timer, and a length of a high level state in the input information within the predetermined time, and for outputting a low level signal if the comparison shows that the length of the low level state is longer than the length of the high level state, and outputting a high level signal if the

comparison shows that the length of the high level state is longer than the length of the low level state.

Both Wakasugi and Sotokawa are silent as to the claimed comparator and therefore, Claim 15 is believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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IN THE DRAWINGS:

Please amend Figure 7 to add the legend "PRIOR ART".